A CDMA Dual-Band Zero-IF Receiver With Integrated LNAs and VCOs in an Advanced SiGe BiCMOS Process

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***Abstract*—This paper describes one of the first dual PCS- and CEL-band CDMA receivers that includes LNAs and VCOs on a single die. The PCS-band LNA achieves a noise figure (NF) of 1.5 dB and IP3 of +7.5 dBm at 16-dB gain. The PCS demodulating mixer achieves an NF of 5 dB, IP3 of +5 dBm and uncalibrated IP2 of +60 dBm. The PCS VCO is capable of −134 dBc/Hz phase noise at 3.9 GHz and 1.25-MHz offset. A copper BiCMOS process was chosen for both performance and cost benefits, compared with lower geometry CMOS.**

***Index Terms*—CDMA, direct conversion, low-noise amplifiers (LNAs), receivers, voltage-controlled oscillators (VCOs).**

I. Introduction

THERE is a clear trend towards CMOS for RFICs due to cost benefits of reduced digital block size and the desire for single-chip integration [1]–[3]. However, most RFIC designers in industry, if given a choice between BiCMOS and CMOS, would choose BiCMOS due to better RF performance and design flexibility. Although the performance gap between BiCMOS and CMOS RF is shrinking, the reduced voltage capability of thin-oxide CMOS devices makes circuit design more challenging and can give increased current consumption where folding becomes necessary.

This paper describes a high-performance CDMA receiver IC designed to be compatible with both legacy and future baseband ASICs, where the legacy analog-to-digital converters (ADCs) are only 6 b. This means that the analog baseband chain must have a wide dynamic range and circuit blocks are consequently physically large. Advanced CMOS processes $\leq$ 0.12 μm are presently expensive per square millimeter of die area and also in nonreturnable expenditure (NRE). In this application, the large ratio of analog-to-digital block area means that 0.25-μm BiCMOS is cheaper than the 0.12-μm CMOS, which would have been required for similar performance. IC process choice and system partitioning are strongly interdependent and require a thorough evaluation at the start of a project.

TABLE I
Minimum and Target System Performance

Parameter (dBm)	CELL Band		PCS Band		Conditions
	EIA98	Target	EIA98	Target	
Sensitivity	-104	-107.5	-104	-107.5	FER=0.005 Max Tx Power
Maximum Input	-25	-25	-25	-25	FER=0.01
Single Tone Desensitization	-30	-27	-40	-37	FER=0.01 Input -101dBm
High Gain Intermodulation	-43	-40	-43	-40	Input -101dBm
Medium Gain Intermodulation	-32	-29	None	-29	Input -90dBm
Low Gain Intermodulation	-21	-18	None	-18	Input -79dBm
Two Tone Blocking	None	-33	None	-33	5MHz and 5.02MHz Tones
RX Band Conducted Noise and Spurious	-76	-79	-76	-79	dBm/MHz

II. System Requirements

Minimum CDMA system requirements are given in ANSI/TIA/EIA-98-D [4] and are summarized in Table I. Target design specifications at room temperature were generally 3 dB tougher than those given by EIA-98-D, to give competitive advantage and customer satisfaction.

Designing a receiver for the CDMA standard is more awkward than designing one for GSM or WCDMA, due to specifications related to single-tone desensitization (STD) [5], [6] and two-tone blocking. STD can be system-partitioned into block specifications for LNA IP3 and VCO phase noise. In this case, the LNA IIP3 requirement was $>$ +7 dBm and VCO phase noise $<$ −128 dBc/Hz at 900-kHz offset from a 3.5-GHz carrier in the CEL band. Two-tone blocking is specified by phone-carrier compliance testing and in this IC leads to requirement on mixer IP2 to be $>$ +55 dBm.

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Challenging system requirements, together with tough market forces, help explain why there are relatively few CDMA chipset providers.

III. Dual-Band Receiver Configuration

LNAs for CDMA CEL and PCS bands have three gain steps to optimize dynamic range and coincide with EIA-98-D intermodulation testing at three input levels. A fixed-gain GPS LNA is also included, for use with a GPS module. CDMA LNA outputs connect to an off-chip dual-band SAW filter that attenuates TX signals and provides single-ended-to-balanced conversion for input to demodulating mixers. Outputs of the two mixers are connected together via MOS switches and then to baseband amplifier input. The baseband amplifier has unity DC gain and selectable 15- or 9-dB gain with a 400-Hz high-pass characteristic set by two external capacitors. The unity-gain low-pass filter provides 615-kHz CDMA bandwidth definition and 65-dB attenuation at 900 kHz by means of a seventh-order elliptic response. A variable gain amplifier (VGA) provides up to 72-dB gain in 3-dB steps with DC compensation and a 400-Hz high-pass response set with two external capacitors. An output 7-b DAC provides compensation for static DC offsets in 2.5-mV steps.

The LO is synthesized by an integer-N-type phase-locked loop (PLL) and includes calibration circuitry for the VCO tuning. The VCO contains two cores, optimized for each band, that operate at 3.5 and 3.9 GHz to reduce leakage in the RX band and allow digital LO dividers for IQ phase accuracy. Power is supplied direct from the battery via on-chip low drop-out voltage regulators (LDOs), and one of these has very low noise for use with VCO. Voltage regulators take 3.1–5.4-V input and produce an output of 2.7 V for block use. The chip is controlled by a three-wire serial bus and serial input–output (SIO) logic is distributed into three blocks to reduce bussing layout area, with some lines gated to reduce interference.

A common bias block provides various output currents for all analog blocks, except for the VCO, which needed very low noise bias. An external trimmed 1.35-V reference was available from the baseband ASIC, so this was used instead of an internal bandgap to reduce bias variation and layout area. Accurate constants with temperature currents were made with 1.35-V reference and an external 1% 27 k resistor by op-amp and mirror configuration. PTAT currents were generated, with a delta VBE circuit and an external 1% 2k7 resistor, to generate a 25-μA unit current. The bias block also generates some currents proportional to internal resistor types, so that process variation is cancelled to first order, for example, in LO voltage swing and baseband IQ output DC offset DACs.

Most blocks have two separate bias registers, each with two control bits, to allow for current versus performance optimization and fast switching between "Normal" and "Economy" mode bias settings. Mode switching between Normal and Economy modes is dependent on gain setting and mode control bits are located in the gain control register to minimize DSP overhead. Normal-mode current consumption is 70 mA and Economy-mode consumption is 55 mA.

The die size is 10.9 mm^2 and the die is packaged in an 81-ball 5×5 mm BGA. The BGA package was chosen for lower cost and higher pin count, compared with QFN. Fig. 1 shows the receiver block diagram.

IV. Block Design and Measurements

A. LNAs

The three-gain CDMA LNA topology used here is very similar to that well described in [6] and was optimized for IC process change from BiCMOS6G to BiCMOS7RF. Three npn transistors with different degeneration are connected at their collectors to provide gain switching, and a low-frequency input trap improves IIP3.

Maximum current was increased to allow higher IIP3, and the process change meant that the PCS band could now be integrated. PCS LNA gain was increased by double bonding the emitter with 90° bond wires connected to adjacent edges of the package to reduce mutual inductance.

A package model for LNA package pins and BGA substrate was extracted by EM simulation with Ansoft Q3D software. LNA simulations were done with Agilent RFDE Harmonic Balance, which allows native support of distributed, frequency-dispersive, printed wiring board (PWB) line features.

Table II summarizes CDMA LNA performance in high gain mode for both bands.

B. Mixers

The previous generation to this IC used an IP2 tuning scheme described in [6] and this had some weakness with temperature sensitivity and LO leakage from DC offset LO waveforms.

After much simulation and test chip investigation of different topologies, it became clear that the basic Gilbert Mixer IIP2 could not be tuned or made sufficiently good with precise layout and that an alternative approach was required. Differential IIP2 depends on both single-ended output IIP2 and balance cancellation. It may be supposed that very good layout matching of 1% could give 40-dB cancellation of IMD2 products; however, simulation showed that, with worst case RF, LO, and device mismatches, the Intermod products themselves were unbalanced in both amplitude and phase by greater than 1-dB amplitude and 10° phase, so that significantly less cancellation is realizable. This means that it is necessary to reduce or filter the IMD2 product before it appears at the output.

The main contribution to IP2 occurs at the Gm input stage due to second-order intermodulation-generating low-frequency IMD2 products, not in the switching mixer stage or due to self-mixing [7], [8]. In general, input stage nonlinearity generates common-mode IMD2 products and LO switching asymmetry generates differential-mode IMD2 products.

The two generic ways to prevent IMD2 products reaching the output are by feedback or high-pass filtering. Filtering by AC coupling the Gm stage to switching stage is very effective, provided high-impedance current sources are used to prevent IMD2 voltages appearing as currents, but gives increased current consumption and noise.

This design reduces IMD2 products by a common-mode feedback loop around the Gm stage bias and functions because IMD2 tone at this point is predominantly a common-mode

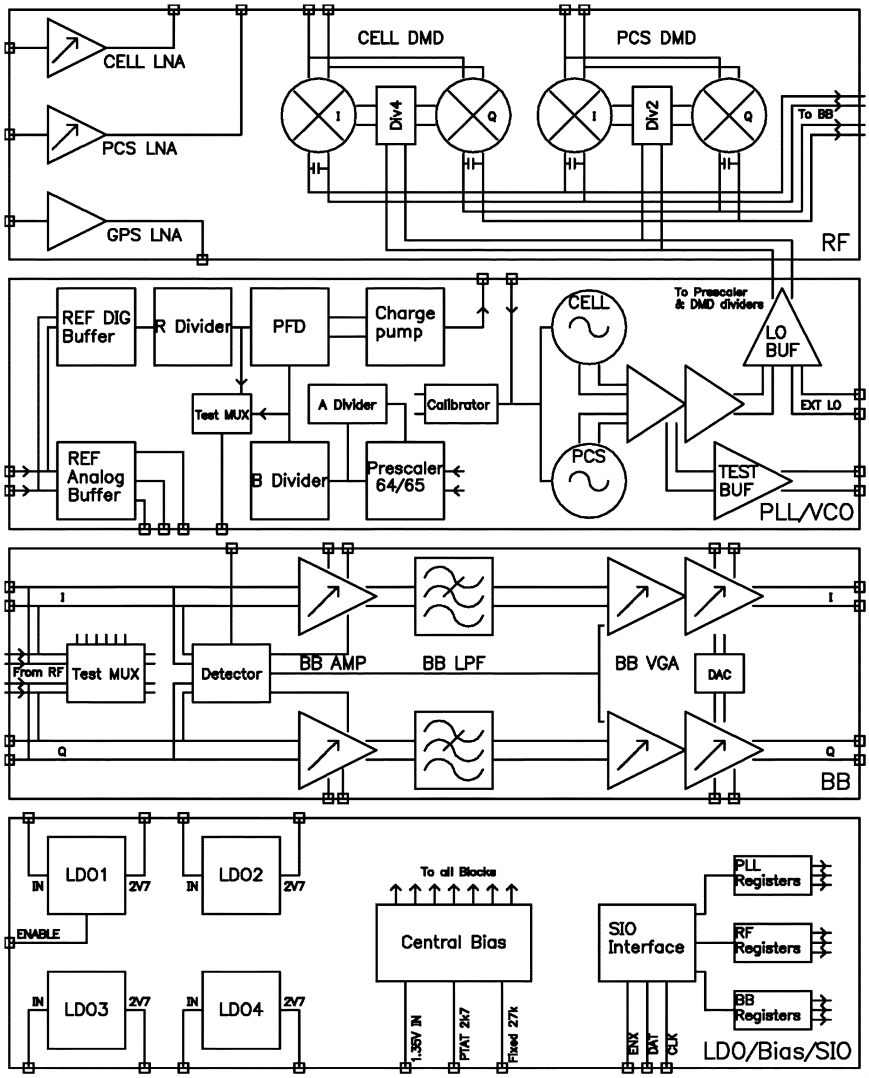

Fig. 1. Receiver block diagram.

TABLE II
LNA MEASURED PERFORMANCE

High Gain Mode	CEL Band	PCS Band
Gain	15dB	16dB
NF	1.3dB	1.5dB
IIP3	+11dBm	+7.5dBm
Current Consumption	8mA	7.5mA

signal. Loop suppression is 30 dB up to 1 MHz and is sufficient for in-band signals and 20-kHz IMD2 tone generated in a 5.0 MHz + 5.02 MHz two-tone test scenario. The same principle but in a different implementation is shown in [9].

The input stage and the switching stage are connected by current-splitting resistors in a "Bixer" configuration [10]. Both I and Q branch currents are used in the single Gm stage and gave a better IIP3 per mA of current consumption, when compared with an alternate design with two parallel Gm stages [6].

Care was also taken with LO generation amplitude, waveform symmetry, and capacitance on emitters of switching mixer devices. Filtering capacitors from mixer outputs to GND were placed adjacent to mixer collector load resistors to locally filter high-frequency signals and reduce the sensitivity of IP2 on output layout routing. Fig. 2 shows a simplified schematic of the IQ mixer.

The mixer was simulated with Agilent RFDE harmonic balance, since this was found to be faster than Cadence PSS. However, the LO waveforms had to be first generated with a transient simulation and captured and converted to spectrum sources for harmonic balance simulation.

IP2 simulated data was examined for both single-ended and differential values. Offsets and mismatches were intentionally added to the RF input, mixer core, LO, and load to obtain realistic worst case simulations. Three sigma DC offsets were calculated to be 0.45 mV at the Gm core and 1.5 mV at the LO driver, and RF input imbalance of 1.5 dB was taken from SAW filter manufacturers data.

Measurements on the mixer block were made on single-ended outputs and differential output and showed that the CEL band had 10-dB lower single-ended IIP2 but better cancellation to give a similar differential value.

It was observed in simulation and measurement that I and Q channels could have IP2 values different by many decibels

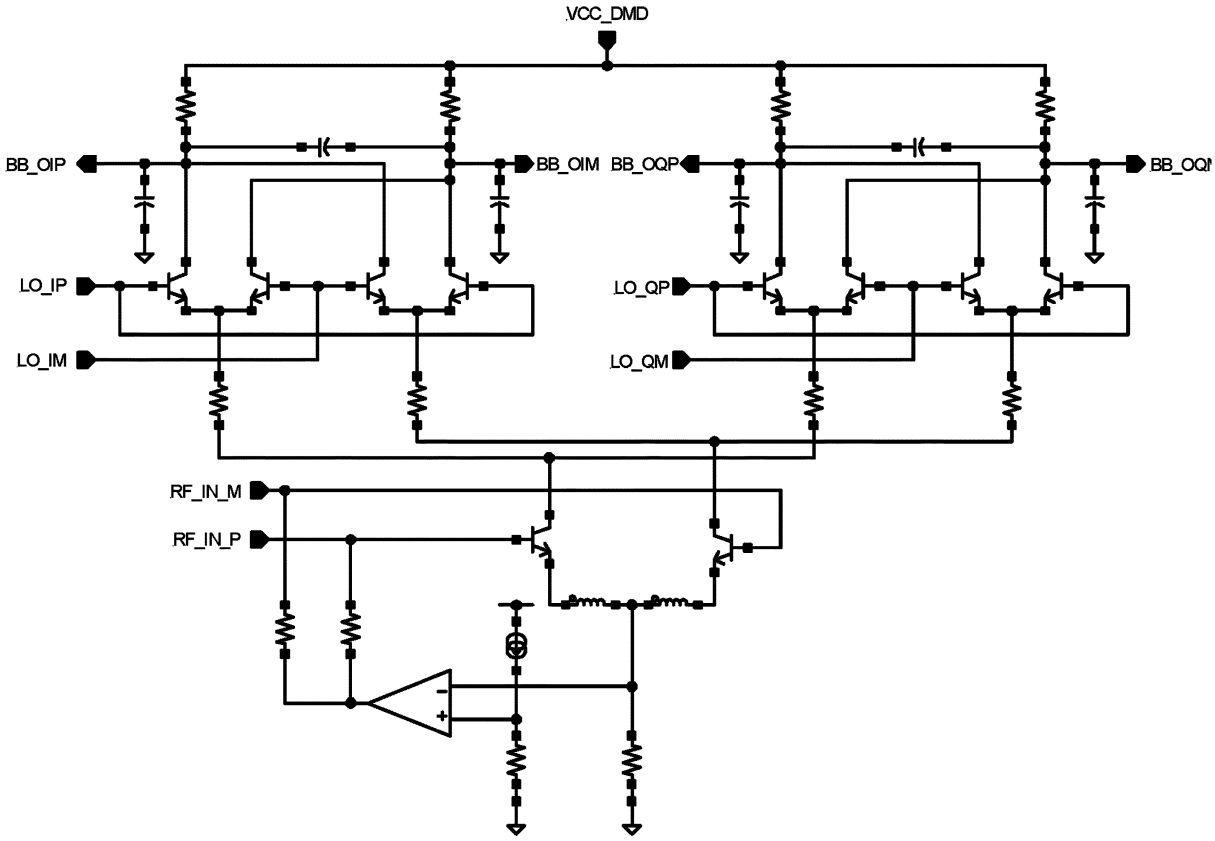

Fig. 2. Mixer schematic.

TABLE III
DEMODULATING MIXER MEASURED PERFORMANCE

	CELL Band	PCS Band
Voltage Gain	13dB	13dB
NF (DSB)	4.5dB	5dB
IIP3	+5dBm	+5.5dBm
IIP2 (single-ended outputs)	+35dBm	+45dBm
IIP2 (I+jQ)	+65dBm	+60dBm
IQ Amplitude Balance	0.2dB	0.2dB
IQ Phase Balance	<1 deg	<1 deg
Current (inc. LO)	20.5mA	19.5mA

and that system performance really depends on the sum of interfering energies, so that an "$I + jQ$" IIP2 metric is a good performance representation, as shown in

$$\mathrm{IIP}_2(I+jQ) \cong 3 - 10\log\left[10^{\frac{-\mathrm{IIP}_{2(I)}}{10}} + 10^{\frac{-\mathrm{IIP}_{2(Q)}}{10}}\right]. \quad (1)$$

This effectively relaxes IIP2 specification in cases where one channel is close to limit, but other channel IIP2 is much higher. Table III summarizes the measured mixer performance for both bands.

C. Baseband

The baseband amplifier provides low-noise 0–18-dB gain in 3-dB steps, although optimized phone AGC just uses 15- and 9-dB settings. The amplifier has unity DC gain, and the high-pass corner is set to 400 Hz by two external 1-μF capacitors; these capacitors have a high value because the impedance level is made low for noise reasons. The supply current of the baseband amplifier was set to minimize the degradation of the RX chain values for IIP3 and IIP2 when compared with raw demodulating mixer performance.

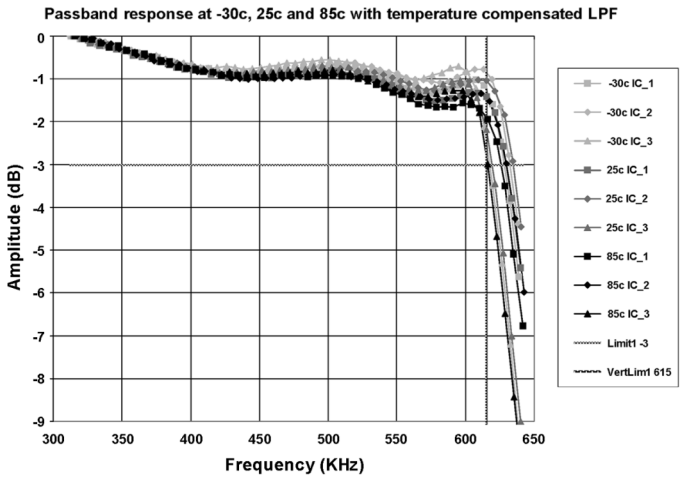

Fig. 3. Temperature-compensated passband response.

To meet the requirements of 65-dB attenuation at 900 kHz and <0.5-dB attenuation at 615 kHz, a seventh-order elliptic filter with a Chebychev passband is used, with one notch falling close to 900 kHz. The filter has 5-b tuning with switched resistors to cover the worst case process. A calibration tone of 640 kHz is generated from 19.2-MHz crystal input frequency

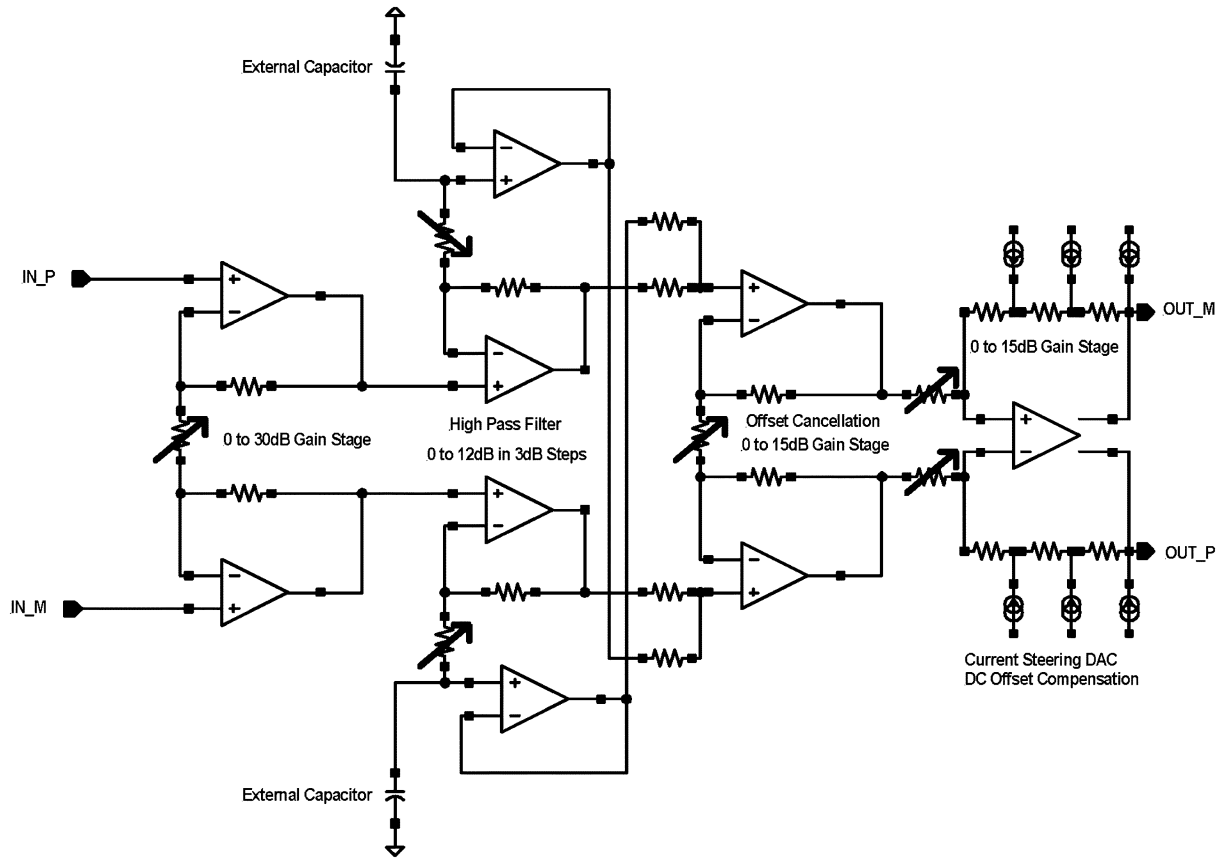

Fig. 4. VGA block diagram.

by a divide-by-30 circuit and a DSP algorithm sets the level of the calibration tone to be between 3 and 6 dB down compared with a wide tuned response. To reduce temperature variation of the corner frequency, two types of poly resistors with opposite temperature coefficients were scaled to give first-order cancellation, and this reduced corner frequency variation to approximately 5 kHz. Resistor temperature coefficients were found to be dependent on exact resistor geometry and a little different from design kit values, so some empirical optimization of the resistor ratio was required.

Fig. 3 shows a plot of the temperature-compensated passband response for three devices, measured with the whole RX chain at -30, 25, and $+85$ c.

The baseband VGA provides up to 72-dB gain in 3-dB steps and consists of three main stages where VGA1 has 0-, 15-, and 30-dB steps, VGA2 has 0-, 6-, 9-, and 12-dB steps, and Output stage has 0-, 15-, and 30-dB steps. Miller compensation capacitors are switched in value as gain is switched to maintain op-amp phase margins. DC compensation is provided with aid of two external 220-nF capacitors which set the high-pass corner to be below 400 Hz. DC offset is sensed at the capacitor nodes by additional op-amps and subtracted from the input response, to improve DC rejection by over 40 dB. The VGA was designed to handle a maximum 20-mV input DC offset and, with a worst case gain step, this gives a 640-mV peak output offset and a 5-ms settling time. However, measured worst case input offset was approximately 5 mV and a software controlled switch is used to speed up capacitor charge/discharge at gain step where offset voltage step is worst case, so measured settling times were less than 1 ms.

A low value of the high-pass corner was found to be necessary for good additive white Gaussian noise (AWGN) performance in measurements and systems simulation, even though a fractional CDMA bandwidth calculation would suggest a few KHz should be sufficient.

A 7-b DAC is connected to feedback resistors of VGA output stage and provides static DC compensation in 2.5-mV steps. Phone software runs a compensation algorithm periodically to tune DAC and so corrects errors over temperature and in Baseband ASIC input.

Fig. 4 shows a VGA block diagram.

A wideband peak level detector is connected to demodulating mixer output and was originally intended to detect strong interfering signal and swap the baseband amplifier and VGA gains by 6 dB to improve linearity. However, it was also beneficial in the AGC to set conditional LNA gain modes and improve linearity in a two-tone test.

Table IV summarizes mixer input to baseband output chain measured performance for both bands.

D. VCOs

Optimum Inductor choice is crucial to good VCO design, with consideration to Q, tuning range, and impedance level with respect to active devices. The inductance of 1 nH in the CEL band and 1.1 nH in PCS was chosen to maximize the voltage swing to 4 V peak-to-peak differential, without

TABLE IV
MIXER TO BASEBAND CHAIN MEASURED PERFORMANCE

	CEL Band	PCS Band
Gain Range	87dB	87dB
Gain variation over Band & Temp.	+1/-1 dB	+2/-2 dB
NF	9dB	9dB
IIP3	+4dBm	+5dBm
IIP2 (I+jQ)	+62dBm	+57dBm
IQ Amplitude Balance	0.3dB	0.3dB
IQ Phase Balance	1 deg	1 deg

saturating the oscillator core or exceeding reliability limits and to give a roughly equal noise contribution as the core-collector current shot noise. The inductor width of 40 μm was chosen to optimize Q at an operating frequency to 25, without adding too much parasitic capacitance. The inductors were available as standard parameterized cells in Design Kit library and are constructed with thick Copper octagonal metallization and grounded patterned polysilicon shield.

Phase noise is very dependent on Kvco and RF voltage across Varactors, but it is also necessary to guarantee a tuning range over IC process corners, and this means that switched tuning is required. A MathCAD sheet was used to calculate Varactor, MIM, and switched capacitance from required tuning range and desired Varactor/MIM voltage ratio.

Total tank Q is the reciprocal sum of individual component Q's, so the Q of each component must be optimized, and great care is needed with layout component placements and interconnect traces to minimize additional routing resistance.

Several small MIM capacitors are used in parallel, to increase capacitor Q to around 200 and to get around IC process restrictions on the number of vias per capacitor. The Varactor was a PN junction type, rather than a MOS type, and the finger width was sized as a compromise between Q and parasitic capacitance.

Three pairs of switched capacitors are binary weighted to give eight tuning steps. nMOS switch devices use 0.25 μm minimum gate length and widths are binary scaled. Absolute nMOS sizes are a compromise between ON-resistance and parasitic capacitance (tuning range). MOS switches connect capacitors directly, rather than via GND, and logic inverters provide gate–source overdrive voltage to ensure that switches are maximally ON or OFF [11].

If a positive frequency versus tune voltage is desired, then the Varactor needs a method for GND bias, and this is awkward in a differential circuit. Some papers have shown resistive bias, but this adds noise and degrades tank Q [12]. The alternative, as was done here, was to inductively choke the RF with two low-area inductors. Choke inductance was optimally set at ten times the tank inductance, and the width was scaled for best overall tank Q. The Varactor GND return tracking was separated and taken to the star point at the VCO GND bond pad to prevent VCO block noise from modulating the varactor. The choke inductors add layout area and some parasitic capacitance but provide a net improvement in phase noise.

Total tank Q is around 18 at mid tuning and degrades slightly when all MOS switches are turned ON. Equivalent series resistance of the tank is about 1.3 Ω, and this low value emphasizes the need for great layout care. The VCO layout was also designed to ensure that there were no parasitic metal loops around inductor, for example in guard bands, since these would act as a magnetic shorted turn and severely degrade Q.

The VCO core features a common mode feedback loop which decreases low-frequency impedance at tail, helps to set optimum bias point, modifies current pulse shape and improves phase noise around 2 dB.

The core's nMOS current source was scaled with a relatively small W/L ratio to minimize 4 KTγGm noise and an RF decoupling capacitor was placed on its drain. It should be noted that using a large W/L ratio will give large Gm and large noise, which can then be inductively filtered as in [13]. The 1-pF capacitor on current source drain reduces RF swing at this node, shapes current pulses, and was found to improve phase noise around 2 dB.

Although there have been some papers published with very good phase-noise CMOS core oscillators [14], this designer found that best performance at 4 GHz was achievable, in this IC process, with a bipolar core due to lower transistor noise. However, the bipolar core suffers from a potential problem over process and temperature, where increasing current gives transistor saturation, causing phase noise to degrade drastically. To prevent saturation and set the optimum operating point, an automatic level control (ALC) is used [12]. An ALC feedback loop detects tank voltage and controls current through the oscillator core. Level detection is done by a differential peak detector does, where voltage on capacitor is a rectified and smoothed version of input waveform [15].

To reduce noise, the peak detector is embedded in an operational transconductance amplifier (OTA) and resistors replace current sources. The input AC level is tapped down by a capacitive divider to prevent reverse-biasing detector transistors on input peaks. DC reference of OTA comes direct from the VCO bandgap, and the DC-bias-to-AC-detector leg is a selectable resistively scaled version of bandgap voltage. NPN devices and bias resistors are matched so that ALC-controlled tank voltage is approximately process-independent [16].

A capacitor to GND on the gate of the current source sets the dominant pole of the ALC loop and filters noise from the ALC.

It should be noted that, although Leeson's equation has proportionality to Q squared, in an ALC voltage-limited system, doubling Q only gives a 3-dB, not a 6-dB, noise benefit because current is halved to maintain same voltage swing.

Fig. 5 shows the VCO core and ALC simplified schematic.

A bandgap reference operating at 0.5 mA provides two low-noise reference voltages needed by the ALC, and this is based on Brokaw topology [17]. The Brokaw topology has reasonable noise performance because NPN devices are resistively degenerated; also, it is not susceptible to base current errors and generates both Vbe and ΔVbe within the same two-transistor cell.

The VCO bias block also provides IC process-compensated bias currents to buffer blocks, so that de-generation voltages are constant, and this avoids risk of up-converted bias noise from overdriven buffers. Bias currents of buffers can be halved for economy mode savings.

Cadence SpectreRF was used for VCO simulation and its PNOISE analysis includes linear additive noise, mixing

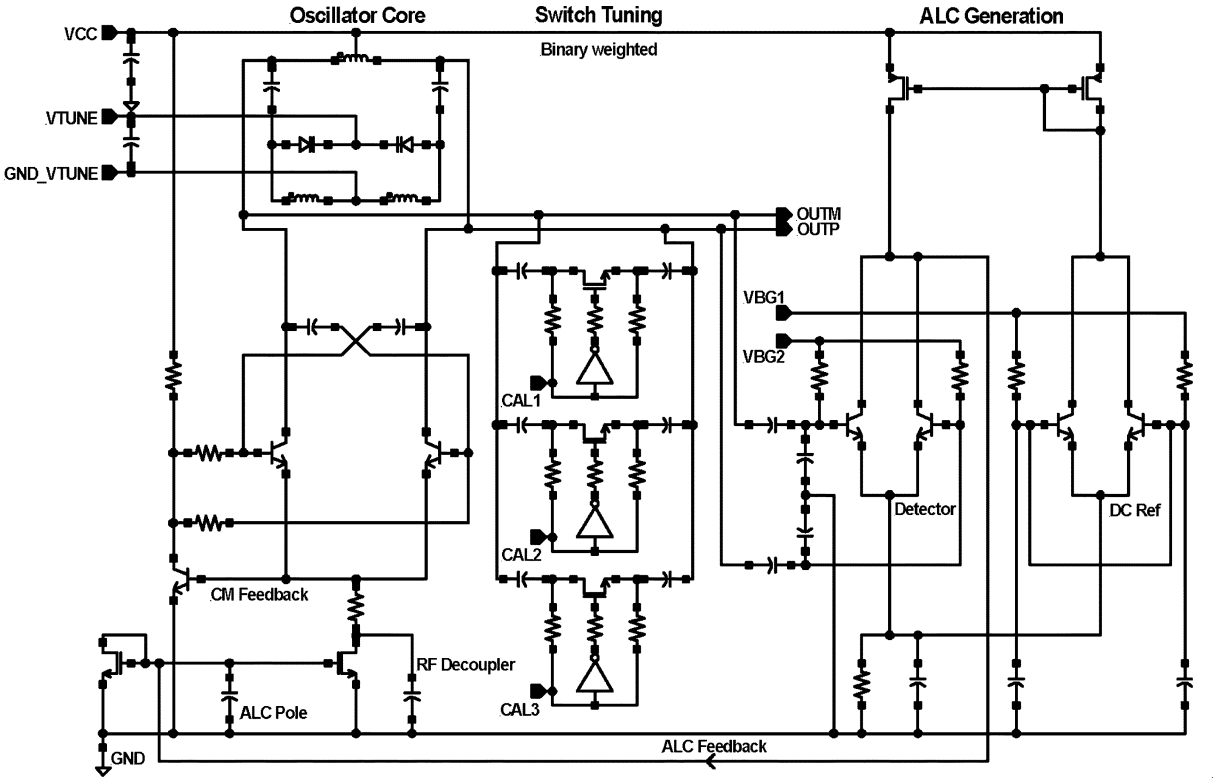

Fig. 5. VCO core and ALC schematic.

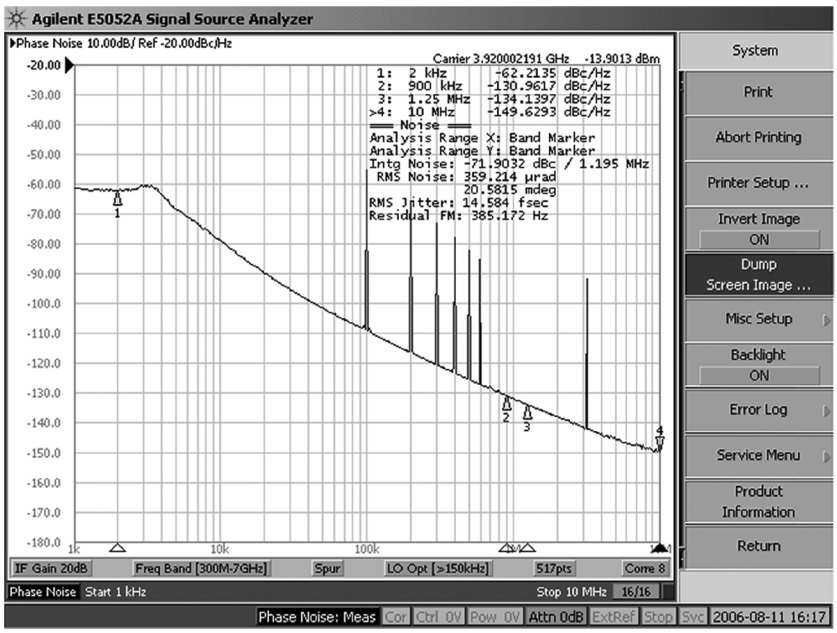

Fig. 6. Measured PCS-band phase noise.

multiplicative noise, and nonlinear time-variant mechanisms. Cadence PNOISE summary was used to examine the top-percentage noise contributors and optimize design. Linear AC analysis and calculator functions for bandwidth and imaginary/real definitions of Q were used to optimize tank Q.

Fig. 6 shows PCS band noise to be −134 dBc/Hz at 1.25-MHz offset and 3.9 GHz. The VCO core current was about 6 mA and gives a phase-noise figure of merit (FOM) for the CEL band of 189 and 192 for the PCS band, which compares well to the best published values [14]. Phase noise is about 3 dB better than that reported for a similar CDMA CMOS VCO, allowing for center frequency [1]. In fact, the phase noise was sufficiently within specifications that the ALC setting could be reduced and current saved.

VCO performance with a PLL is summarized for both bands in Table V.

TABLE V
VCO WITH PLL MEASURED PERFORMANCE

	CEL Band	PCS Band
Carrier Frequency	3526MHz	3920MHz
Offset Frequency	900kHz	1.25MHz
Phase Noise	-131.5dBc/Hz	-134dBc/Hz
FOM	189	192
Core Current	6mA	6mA
Normal Mode VCO Current	15mA	15mA
Economy Mode VCO Current	11mA	11mA

E. PLL

The settling time requirement for a CDMA PLL is 2.5 ms, which is relatively slow compared with GSM, and this means that an integer-N PLL with 3-kHz bandwidth is adequate. In-band phase noise (1–615 kHz) sets the ultimate RX signal to noise obtainable, and -24 dBc at an LO frequency was deemed to be adequate for evolution-data-optimized (EV-DO) application. It should be noted that tougher in-band phase noise would have required a fractional-N PLL.

Although there have been several papers promoting a phase-switching-type prescaler, it can have problems with waveform asymmetry causing subharmonic reference spurs on the VCO spectrum [18]. In this design, a conventional 64/65 prescaler with a synchronous 4/5 bipolar core was used and was optimized for current consumption with the aid of an internal DC feedback loop to give constant voltage swings. It should be noted that the 4/5 divider core has four potential outputs, each separated by 90°, but only one of these will give the minimum clock-to-modulus control delay when connected to A and B counters; this issue can cause a PLL to fail at certain channels but is rarely mentioned in the literature.

Counters for R, A, and B dividers, as shown in Fig. 1, were designed to be pseudosynchronous with resynchronization to minimize current consumption and accumulated phase noise. The duty cycle was also made low to reduce high-frequency energy for spur reduction reasons.

The VCO design required a low Kvco for phase-noise reasons and, to guarantee tuning range over worst case process and conditions, a high-voltage charge-pump was required. The charge-pump was designed with high-voltage bipolar devices, incorporated beta compensation, and provided $<10\%$ mismatch within 0.5–4.1-V output range. The reference spur level was below -55 dBc.

Charge-pump current is 1.0 mA in the CEL band and 1.33 mA in the PCS band to compensate for differences in N and give the same loop bandwidth in both bands; Kvco is same for CEL and PCS VCOs.

The PLL includes calibration circuitry to set VCO 3-b tuning at each requested channel change. In this scheme, the loop filter is precharged to the middle voltage of frequency versus Vtune characteristic and tuning CAL bits are set to mid values. A phase comparator measures if the main divider output is high or low with respect to the reference divider, and a successive approximation register (SAR) halves the CAL bit count at each comparison frequency interval to find the correct 3-b CAL code in four reference frequency periods. After calibration, the loop is closed and the PLL locks quickly since the tune voltage is effectively precharged. Requirements for this scheme are that the reference divider, main divider, and PFD must be reset and that VCO tuning curves must overlap.

V. TOP-LEVEL VERIFICATION AND IC TESTABILITY

The IC was verified to be functionally correct from SIO programming to the baseband output at the top level, in external LO mode, using HSIM transient simulation. Digital logic was represented at full transistor level, but simulator accuracy was set more loosely for those blocks. RF signals were applied after programming and DC stabilization to optimize simulation time, and useful data were obtainable overnight. Cadence Spectre DC and transient analysis was also used at the top level, but with voltage source representation of internal logic lines. With these simulation tools, it was possible to catch two previously unseen power-up and oscillation problems before GDSII tapeout.

A mass-production IC needs to be thoroughly testable for both performance at the development stage and for manufacturing defects at the production stage. Testability needs to be designed in at the start to avoid costly redesign, and, in this case, the following features were included; pin access to mixer outputs and baseband inputs, baseband chain multiplex switching, PLL divider test output, external LO input, LDO Kelvin access, VCO test buffer output, and IC version number readable via serial input–output interface. Test features were also verified by simulation to be functionally correct.

Total device cost can be partitioned approximately equally between die size, package, and testing, so that it is necessary to minimize test time while still providing adequate test coverage. Adding test pins, test modes, read-back registers, and designing out calibrations speeds up test time and eases the bench test.

VI. BICMOS7RF PROCESS

This IC was fabricated on STMicroelectronics' BiCMOS7RF process, which contains many state-of-the-art performance features. Very low noise, 60-GHz Ft carbon-doped SiGe NPN transistors are available, which benefited every block, particularly LNAs, VCOs, and mixers, and enabled integration of the PCS-band LNA. High-voltage (5-V) variants of this device were also used, for example, in the PLL charge-pump.

Digital library with 0.25-μm geometry CMOS enabled shrinking of digital control blocks and PLL dividers from previous-generation ICs described in [6]. A 0.35-μm low-leakage digital library was also available and used in analog blocks.

Top-layer 4-μm-thick Copper with 5-mΩ/sq resistivity was used for inductors, RF, and supply routing. This layer had a factor of 10 less resistivity than the M2–M4 layers and allows choices of high Q or low-area inductors and low resistance or thinner routing.

High-Q MIM capacitors at the M4–M5 levels provide 5-fF/μm^2 density and are stackable above other devices, as in the LPF.

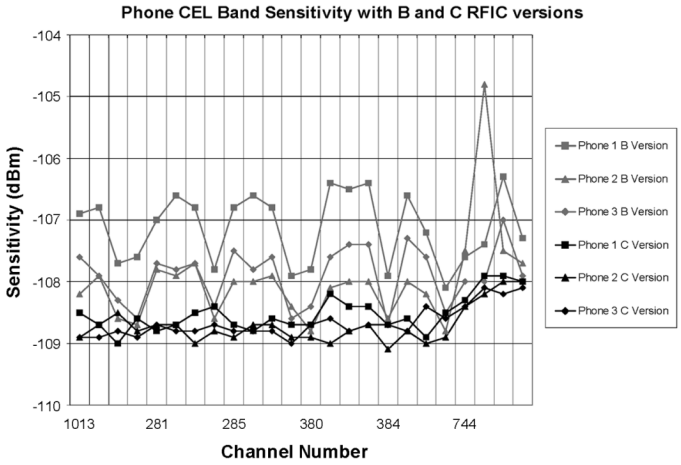

Fig. 7. Phone sensitivity with and without prescaler spurs.

Deep trench isolation (DTI) was used at both the device level for reduced capacitance and at the block level for isolation. LO leakage is critical in direct conversion, and DTI helped make leakage 20 dB better than specifications. It was also crucial in reducing system problems, as described in Section VII.

VII. System Interference Issues and ESD

The first version of this IC had a problem where PLL out-of-band phase noise could increase up to 6 dB, depending on CDMA input and gain levels, due to coupling from baseband blocks to VCO. To fix this, a DTI/GND/DTI sandwich was placed around the VCO, with GND taken to a dedicated pin. There was a cut in isolating GND to prevent a metal ring, giving a shorted turn degradation of the VCO inductor Q. With this second full-mask iteration, measured phase-noise degradation became less than 0.2 dB over the whole CDMA dynamic range.

Another system-type problem was found later after an all-channel sensitivity sweep, where spurs generated by the PLL prescaler fell into the CEL RF band and desensitized the receiver by up to 2.0 dB. Spurs were synchronous with modulus control signal and generated 120-kHz comb at the CEL band which gave, depending on the RF channel number, 30- or 60-kHz baseband spurs, with every fourth channel clean. RF spurs were picked up in the LNA and mixer, but the VCO spectrum was clean. To fix this problem, several steps were taken; a second isolating buffer was added to the prescaler input, substrate coupling was reduced with a DTI/GND/DTI sandwich added around the PLL with continuous GND to short the magnetic field, big filtering capacitors (BFCs) and 10-Ω series resistors were added to analog and digital prescaler supplies to make high-frequency current circulate locally rather than through bond wires. With this third full-mask iteration, the spur level measured at the baseband output was reduced 15 dB, and no receiver desensitization was measurable in phone. Fig. 7 shows measured sensitivity plots for three phones with B-version ICs and then remeasured with final C-version ICs.

The first version of this IC was found to have some ESD weakness, and it became apparent that device voltage limits for the more modern IC process had decreased but ESD pad design and choice had not kept track. Voltage transients on each pad type were simulated with a representation of the human body model (HBM), and then all unique current paths were analyzed to determine the total voltage that would be seen by a device connected to pad; these voltages were then compared with device maximum ratings. To reduce ESD transient voltages, more clamps were added around the ring to reduce IR drops, additional series resistance was added to some MOS gate connections, and some pads were changed with a number of positive supply diodes set as the best compromise between ESD performance and false power-up/leakage scenarios. After these changes, a 1-kV HBM rating was obtainable.

TABLE VI
Measured System Performance

Parameter (dBm)	CELL Band	PCS Band	Conditions
Sensitivity	-108	-107.5	FER=0.005 Max Tx Power
Maximum Input	-25	-25	FER=0.01
Single Tone Desensitization	-26	-26	FER=0.01 Input -101dBm
High Gain Intermodulation	-37	-38	Input -101dBm
Medium Gain Intermodulation	-27	-28.5	Input -90dBm
Low Gain Intermodulation	-16.5	-16.5	Input -79dBm
Two Tone Blocking	-29	-29	5MHz and 5.02MHz Tones
RX Band Conducted Noise and Spurious	<-100	<-100	dBm/MHz

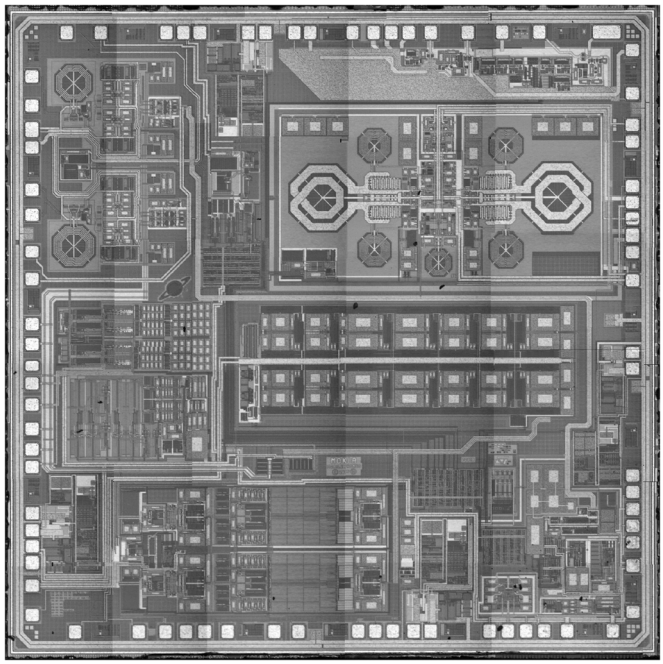

Fig. 8. Die microphotograph.

VIII. Conclusion

This paper describes one of the first mass production dual CEL–PCS-band CDMA receiver ICs with integrated LNAs and

VCOs. Previously published CDMA receivers have been either CEL-band only or required an external LO signal.

The IC uses circuit topology enhancements for mixer, VCO, and VGA blocks and utilizes the advantages of an advanced BiCMOS process to meet tough performance requirements.

The measured system performance is summarized in Table VI and shows good margin to EIA-98-D.

System interference problems, which are a risk with increased integration levels, were found and were overcome with layout features and circuit changes.

ESD problems, which are a risk with IC-process feature-size reduction, were found and were overcome with pad and circuit changes.

Also, supply current reduction, through the use of "Normal" and "Economy" modes, have contributed to an outstanding phone standby time of 13 days.

Fig. 8 shows a microphotograph of the die in a wafer.

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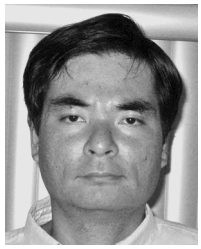

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Peter Borowitz, photograph and biography not available at the time of publication.

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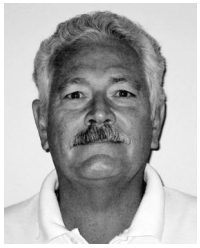

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